
(Português em Português).(English) External links Category:Numeracy Category:Numeracy in mathematicsRecently, a patent specification called as two-dimensional (2D) stacked memory technology has been proposed, in which a plurality of memory cells are disposed in a direction (memory cell column) perpendicular to a word line and are sequentially disposed in a direction (memory cell row) perpendicular to the memory cell column. This kind of two-dimensional (2D) stacked memory can be configured of a combination of an N-type memory cell and a P-type memory cell, in which the N-type memory cell includes one source/drain region of a first conductivity type and one source/drain region of a second conductivity type, and the P-type memory cell includes one source/drain region of the first conductivity type and one source/drain region of the second conductivity type. In this case, the source/drain regions of the second conductivity type in the N-type memory cell and the P-type memory cell are typically connected with a bit line BL, which has a first voltage level, and a word line WL, which has a second voltage level, respectively. On the other hand, the source/drain regions of the first conductivity type are typically connected with a source line SL, which has a third voltage level. Therefore, the source/drain regions of the second conductivity type are electrically connected to the source line SL, which has the third voltage level, in the P-type memory cell. Furthermore, the N-type memory cell, the P-type memory cell, the bit line BL, the word line WL, and the source line SL are typically disposed by an interlayer insulating film. In the case of this kind of 2D stacked memory, in order to prevent operation errors and ensure reliability, a P-type memory cell that includes an oxide film is provided between a memory cell and a contact (connection) to a bit line (contact to the bit line BL) that is adjacent to the memory cell, in which the oxide film is typically formed on a semiconductor substrate (see JP-A-2009-27623, for example). JP-A-2009-27623 discloses a transistor element and a method for manufacturing the same. In the transistor element disclosed in JP-A-2009-27623, 82157476af

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